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HEWLETT-PACKARD COMPANY  
Intellectual Property Administration  
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EXAMINER

MASON, DONNA K

ART UNIT PAPER NUMBER

2111

DATE MAILED: 11/05/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

# Office Action Summary

Application No.

09/918,024

Applicant(s)

ERICKSON ET AL.

Examiner

Donna K. Mason

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

## Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☒ Responsive to communication(s) filed on 17 June 2004.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 6,9 and 11-21 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 6,9 and 11-21 is/are rejected.
- 7) ☒ Claim(s) 14 and 21 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 30 July 2001 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

## Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
  - ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

## Attachment(s)

- ☒ Notice of References Cited (PTO-892)
- ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_
- ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_
- ☐ Notice of Informal Patent Application (PTO-152)
- ☐ Other: \_\_\_\_\_

## **DETAILED ACTION**

### ***Claim Objections***

1. Claim 14 is objected to because of the following informalities: in line 1, "an" should be changed to --a--.
2. Claim 21 is objected to because of the following informalities: in line 4, insert --.-- (a period) after "buffer". Appropriate correction is required.
3. Appropriate correction is required. See 37 CFR 1.75.

### ***Claim Rejections - 35 USC § 112***

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:  
  
The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.
5. Claims 6, 9, and 11-21 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.
6. Claim 9 recites the limitation "apparatus" in line 3. For clarity, it is recommended that --an-- be inserted before "apparatus".
7. Claim 9 recites the limitation "a particular target bus port" in line 4. It is unclear whether this recitation refers to the previously recited "a particular target serial bus port" in line 3.
8. Claim 9 recites the limitation "the first bus interface" in line 5. There is insufficient antecedent basis for this limitation in the claim.

9. Claim 9 recites the limitation "apparatus" in line 9. For clarity, it is recommended that --an-- be inserted before "apparatus".

10. Claim 9 recites the limitation "the particular bus port" in line 11. There is insufficient antecedent basis for this limitation in the claim.

11. Applicant is advised to review *all of the claims* to determine whether each acronym has been spelled out at the first occurrence of the acronym *in the base claim of each group of claims*. For example, each of the terms of the acronym "JTAG" (see claim 9, line 6) should be spelled out at the first occurrence of the acronym in the base claim 9. Similarly, each of the terms of the acronyms "IIC" (e.g., claim 11), "FIFO" (e.g. claim 12), "EEPROM" (e.g., claims 14 and 19), and "FPGA" (e.g., claim 17 and 19) should be spelled out at the first occurrence of each acronym in its respective base claims.

12. Claim 12 recites the limitation "the first bus interface" in line 2. There is insufficient antecedent basis for this limitation in the claim.

13. Claim 12 recites the limitation "bus ports" in line 4. This limitation should be deleted because it appears to be a duplicate of the previously recited "bus port" in line 3.

14. Claim 13 recites the limitation "the particular target serial bus" in lines 3-4. There is insufficient antecedent basis for this limitation in the claim.

15. Claim 15 recites the limitation "a serial bus port" in lines 1-2. It is unclear whether "a serial bus port" refers to the previously recited "particular target serial bus port" or another one of the previously recited "plurality of target serial bus ports".

16. Claim 15 recites the limitation "the serial bus" in line 3. There is insufficient antecedent basis for this limitation in the claim.
17. Claim 16 recites the limitation "the target serial busses" in line 2. There is insufficient antecedent basis for this limitation in the claim.
18. Claim 18 recites the limitation "apparatus" in line 8. For clarity, it is recommended that --an-- be inserted before "apparatus".
19. Claim 18 recites the limitation "the first bus interface" in line 9. There is insufficient antecedent basis for this limitation in the claim.
20. Claim 19 recites the limitation "selected" in both lines 3 and 5. Because claim 19 is a new claim, "selected" should not be underlined.
21. Claims 6, 20 and 21 inherit the deficiencies of their respective base claims.
22. Applicant is advised to carefully review all of the claims, and any changes made to the claims, for 35 USC 112, second paragraph problems, and to make corrections, where appropriate.

### ***Claim Rejections - 35 USC § 102***

23. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

24. Claims 9 and 11 are rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 5,933,614 to Tavallaei, et al. ("Tavallaei").

With regard to claim 9, Tavallaei discloses a bus bridge (Fig. 10, item 700) including: a first serial bus interface (Fig. 10, item 710), the first serial bus interface operable as a bus slave; apparatus (not shown, *but see* column 25, lines 66-67 to column 26, lines 1-2) for selecting a particular target serial bus port of a plurality of target serial bus ports, the apparatus for selecting a particular target [serial] bus port addressable through the first bus interface, where the plurality of target [serial bus] ports includes at least two JTAG bus ports (Fig. 10, item 705; column 25, lines 66-67 to column 26, lines 1-2); apparatus for transferring information between the first serial bus interface and the particular target serial bus port, the apparatus for transferring information operable as a bus master on the particular [target serial] bus port (column 25, lines 60-63; and see bus connecting items 705 and 710).

With regard to claim 11, Tavallaei discloses the bus bridge where the first serial bus interface is an IIC bus interface (Fig. 10, item 710; column 23, lines 37-57).

Therefore, Tavallaei reads on the invention as specified in claims 9 and 11.

25. Claims 6, 9, 11, 12 and 18 are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent No. 6,684,362 to Currier, et al. ("Currier").

With regard to claim 9, Currier discloses a bus bridge (Fig. 1, item 100) including: a first serial bus interface (Fig. 1, item 104), the first serial bus interface operable as a

bus slave; apparatus (Fig. 1, item 108) for selecting a particular target serial bus port of a plurality of target serial bus ports (Fig. 1, items 112 and 110), the apparatus for selecting a particular target [serial] bus port addressable through the first bus interface, where the plurality of target [serial bus] ports includes at least two JTAG bus; apparatus (Fig. 1, item 102 and Fig. 2, item 200) for transferring information between the first serial bus interface and the particular target serial bus port, the apparatus for transferring information operable as a bus master on the particular [target serial] bus port (column 3, lines 46-65).

With regard to claim 11, Currier discloses the bus bridge where the first serial bus interface is an IIC bus interface (Fig. 1, item 104).

With regard to claim 12, Currier discloses the bus bridge where the apparatus for transferring information between the first [serial] bus interface and the particular target serial bus port includes at least one FIFO (Fig. 2, item 201).

With regard to claim 18, Currier discloses a bus bridge (Fig. 1, item 100) including: a first serial bus interface (Fig. 1, item 104), the first serial bus interface operable as a bus slave; a target serial bus interface (Fig. 1, item 108) including a plurality of target serial bus ports (Fig. 1, items 112, and 110); selection logic (Fig. 1, item 113) coupled such that the first serial bus interface can designate a selected target serial bus port of the plurality of target serial bus ports, and where the target serial bus interface is operable as a bus master on the selected target serial bus port; and [an] apparatus (Fig. 1, item 102 and Fig. 2, item 200) coupling the serial bus interface to the target serial bus interface, such that commands received by the first bus interface are

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capable of causing execution of commands by the target serial bus interface on the selected target serial bus port, the apparatus coupling the first serial bus interface to the target serial bus interface further including at least one First-in-First-Out (FIFO) buffer (Fig. 2, item 201) and a status register (Fig. 2, item 202) having flags for detecting data in the at least one FIFO buffer; wherein the target serial bus interface is a Joint Test Action Group (JTAG) bus interface (Fig. 1, item 108).

With regard to claim 6, Currier discloses the bus bridge where the first serial bus interface is an Inter-Integrated Circuit (IIC) bus interface (Fig. 1, item 104).

Therefore, Currier reads on the invention as specified in claims 6, 9, 11, 12 and 18.

### ***Claim Rejections - 35 USC § 103***

26. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

27. Claims 12 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tavallaei in view of International Publication No. WO 97/15011 by Ruddy, et al. ("Ruddy").

As described above in the 35 U.S.C. 102(b) rejection, Tavallaei discloses all the features of claims 9 and 11.

With regard to claims 12 and 13, Tavallaei does not expressly disclose the bus bridge where the apparatus for transferring information between the first bus interface and the particular target serial bus port includes at least one FIFO; or where the bus bridge further includes a bypass mechanism such that data may be communicated between the first serial bus interface and the particular target serial bus [port] without using the at least one FIFO.

Ruddy discloses a bus bridge (Fig. 1, item 100) where the apparatus for transferring information between the first [serial] bus interface (Fig. 1, item 102) and the particular target serial bus port (Fig. 1, item 116) includes at least one FIFO (Fig. 1, items 126 and 128); or where the bus bridge further includes a bypass mechanism such that data may be communicated between the first serial bus interface and the particular target serial bus [port] without using the at least one FIFO (see path in Fig. 1, from 107 to 110, and then from 110 to 105).

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to combine Ruddy with Tavallei. The suggestion or motivation for doing so would have been to enhance overall system throughput by significantly reducing the number of interrupts to be processed by the particular target serial bus port (page 13, line 30 to page 14, lines 1-2).

Therefore, it would have been obvious to combine Ruddy with Tavallaei to obtain the invention as specified in claims 12 and 13.

28. Claims 14-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tavallaei in view of Ruddy as applied to claims 12 and 13 above, and further in view of Vorgert.

With regard to claims 14-16, Tavallaei in view of Ruddy discloses all the features of claims 12 and 13.

Tavallaei in view of Ruddy does not expressly disclose the bus bridge implemented in a Field Programmable Gate Array (FPGA) having an associated EEPROM for storing configuration code; where a serial bus port of the target serial ports is coupled to the EEPROM, and where the EEPROM may be erased and written through the serial bus; and where the serial bus port coupled to the EEPROM is also coupled to a configuration header, as recited in claims 14-16.

Carrier discloses the bus bridge implemented in a Field Programmable Gate Array (FPGA) having an associated EEPROM for storing configuration code; where a serial bus port of the target serial ports is coupled to the EEPROM, and where the EEPROM may be erased and written through the serial bus; and where the serial bus port coupled to the EEPROM is also coupled to a configuration header.

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to implement the bus bridge of Tavallaei in view of Ruddy in the bus bridge FPGA of Vorgert. The suggestion or motivation for doing so would have been to provide a method of reprogramming an EEPROM device without the need for special hardware, interruption of normal system operation during the reprogramming process, or special interfaces (column 1, lines 35-39).

Therefore, it would have been obvious to combine Vorgert with Tavallaei in view of Ruddy to obtain the invention as specified in claims 14-16.

29. Claims 17 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Carrier in view of U.S. Patent No. 6,137,738 to Vorgert.

With regard to claims 17 and 19, Carrier discloses all the features of claims 9, 11, and 18, as discussed above with regard to the 35 USC 102(e) rejection of those claims.

Carrier does not expressly disclose the bus bridge implemented in a bus bridge FPGA having an EEPROM associated therewith for storing configuration code, where a selected serial bus port of the target serial bus ports is coupled to the EEPROM associated with the bus bridge FPGA, and where the EEPROM associated with the bus bridge FPGA may be erased and written through the selected target serial bus port, thereby permitting modification of the bus bridge, as recited in claims 17 and 19.

Vorgert discloses a bus bridge FPGA (Fig. 1, item 12) having an EEPROM (Fig. 1, item 10) associated therewith for storing configuration code (column 2, lines 16-20), where a serial bus port (Fig. 1, item 20) is coupled to the EEPROM associated with the bus bridge FPGA, and where the EEPROM associated with the bus bridge FPGA may be erased and written through the selected target serial bus port, thereby permitting modification of the bus bridge (*see generally*, column 1, lines 7-10; column 2, lines 15-67 to column 3, lines 1-63).

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to implement the bus bridge of Carrier in the bus bridge FPGA of Vorgert.

The suggestion or motivation for doing so would have been to provide a method of reprogramming an EEPROM device without the need for special hardware, interruption of normal system operation during the reprogramming process, or special interfaces (column 1, lines 35-39).

Therefore, it would have been obvious to combine Vorgert with Carrier to obtain the invention as specified in claims 17 and 19.

30. Claims 20 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Carrier in view of Vorgert as applied to claims 17 and 19 above, and further in view of Ruddy.

With regard to claims 20 and 21, Carrier in view of Vorgert discloses all the features of 17 and 19 as discussed above with regard to the 35 USC 103(a) rejection of those claims.

Carrier in view of Vorgert does not expressly disclose the bus bridge, where the apparatus for transferring information has a bypass mode such that the EEPROM associated with the bus bridge FPGA can be erased and written without using the at least one FIFO buffer, as recited in claims 20 and 21.

Ruddy discloses a bus bridge (Fig. 1, item 100), where the apparatus for transferring information has a bypass mode such that the EEPROM associated with the bus bridge FPGA can be erased and written without using the at least one FIFO buffer (see path in Fig. 1, from 107 to 110, and then from 110 to 105).

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to combine Ruddy with Currier in view of Vorgert. The suggestion or motivation for doing so would have been to enhance overall system throughput by significantly reducing the number of interrupts to be processed by the particular target serial bus port (page 13, line 30 to page 14, lines 1-2).

Therefore, it would have been obvious to combine Ruddy with Currier in view of Vorgert to obtain the invention as specified in claims 20 and 21.

### ***Response to Arguments***

31. Applicant's arguments, see pages 9-12, filed June 17, 2004, with respect to the rejections of claim 9 under 35 USC 102(e), and claims 6, 11, and 17 under 35 USC 103(a) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Tavallaei, Ruddy, Currier, and Vorgert.

The Examiner is persuaded that Pawlowski does not expressly disclose a serial-to-serial bus interface as claimed. However, Tavallaei, Ruddy, and Currier each teach this feature.

Although Jeddelloh discloses that "expansion buses other than PCI buses and ISA buses . . . may be used, the Examiner is persuaded that Jeddelloh does not expressly disclose a serial-to-serial bus interface as claimed. However, Tavallaei, Ruddy, and Currier each teach this feature.

***Conclusion***

32. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the date of this final action.

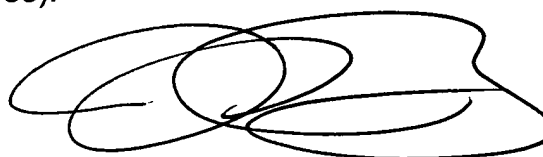
Any inquiry concerning this communication or earlier communications from the examiner should be directed to Donna K. Mason whose telephone number is (571) 272-3629. The examiner can normally be reached on Monday - Friday, 8:30am - 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark H. Rinehart can be reached on (571) 272-3632. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DKM

A handwritten signature in black ink, consisting of several overlapping loops and a long horizontal stroke at the bottom.

**MARK H. RINEHART  
SUPERVISORY PATENT EXAMINER  
TECHNOLOGY CENTER 2100**